IN THE CLAIMS:

Please cancel claim 41 and amend the claims as follows:

1. (Original) A method of operating a control circuit in a multiple data rate memory device, comprising, within a given clock period:

driving first data on a data bus;

transmitting, via a first signal path, a strobe signal to a receiving circuit indicating the validity of the first data on the data bus;

receiving a return signal indicating an assumed arrival of the strobe signal at the receiving circuit; and

in response to receiving the return signal, driving second data on the data bus.

2. (Original) The method of claim 1, wherein driving the first data and the second data on the data bus comprises enabling a driver to drive the data.

3. (Original) The method of claim 1, wherein the data bus is an internal data bus of the multiple data rate memory device.

4. (Original) The method of claim 1, wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory (DDR SDRAM).

5. (Original) The method of claim 1, wherein a duration of time between issuing the strobe signal and receiving the return signal is at least as long as a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit.

6. (Original) The method of claim 1, wherein a duration of time between issuing the strobe signal and receiving the return signal is substantially equal to a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit.

7. (Original) The method of claim 1, wherein the return signal is the strobe signal.

8. (Original) The method of claim 1, further comprising generating the return signal by the receiving circuit.

9. (Original) The method of claim 8, wherein generating the return signal comprises buffering the strobe signal.

10. (Currently Amended) A method of operating a multiple date rate memory device, comprising, within a given clock period:

(a) driving a first data on a data bus;

(b) issuing a strobe signal from a controller;

(c) receiving, by a receiving circuit, the strobe signal a period of time after issuing the strobe signal;

(d) in response to receiving the strobe signal by the receiving circuit, latching in the first data from the data bus;

(e) receiving, by the controller, the strobe signal a period of time after issuing the strobe signal; and

(f) in response to receiving the strobe signal by the controller, driving a second data on [[a]]the data bus.

11. (Original) The method of claim 10, wherein (a)-(f) are performed bidirectionally over the data bus.

12. (Original) The method of claim 10, wherein the strobe signal is propagated to the receiving circuit on a first path and propagated to the controller on a second path, and wherein only a portion of each path shares a common line.

13. (Original) The method of claim 10, wherein the strobe signal is propagated to the receiving circuit on a first path and propagated to the controller on a second path, and wherein lengths of the first and second paths are substantially the same.

14. (Original) The method of claim 10, further comprising:

(g) latching the second data in from the data bus.

15. (Original) The method of claim 10, wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory (DDR SDRAM).

16. (Original) A method of operating a multiple date rate memory device, comprising, within a given clock period:

(1) by a driver controller:

driving first data on a data bus;

transmitting a data strobe signal to a receiver via a forward signal path;

receiving the data strobe signal via a return signal path; and

in response to receiving the strobe signal, driving second data on the data bus; and

(2) by a receiver:

receiving the strobe signal via the forward signal path; and

in response to receiving the strobe signal, latching the first data in from the data bus.

17. (Original) The method of claim 16, wherein the forward signal path is defined on a first line and the return signal path is defined on a second line branching from the first line.

18. (Original) A method of operating a control circuit in a multiple date rate memory device, comprising, within a given clock period:

enabling a driver to drive a first data on a data bus;

issuing a strobe signal to a receiving circuit via a forward signal path to indicate the presence of the first data on the data bus;

receiving the strobe signal via a return signal path, wherein receipt of the strobe signal indicates an assumed arrival of the strobe signal at the receiving circuit via the forward signal path; and

in response to receiving the strobe signal, enabling a driver to drive a second data on the data bus.

19. (Original) The method of claim 18, wherein a period of time between issuing the strobe signal and receiving the strobe signal is at least as long as a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit.

20. (Original) The method of claim 18, wherein a period of time between issuing the strobe signal and receiving the strobe signal is substantially equal to a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit.

21. (Original) The method of claim 18, wherein receiving the strobe signal by the control circuit occurs substantially simultaneously with receipt of the strobe signal by the receiving circuit.

22. (Original) The method of claim 18, wherein the data bus is an internal data bus of the multiple data rate memory device.

23. (Original) The method of claim 18, further comprising, within the given clock period, driving the first data on the data bus.

24. (Original) The method of claim 18, wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory.

25. (Original) The method of claim 18, wherein the strobe signal is issued on a first line and is received on a second line, wherein the first line and the second line form at least part of a round-trip path for propagating the strobe signal.

26. (Original) The method of claim 25, wherein the first line is coupled to the receiving circuit.

27. (Original) A multiple data rate memory device, comprising:

a controller configured to generate one or more driver-enable signals and a strobing clock signal;

a data bus;

a driver circuit configured to drive a first data and a second data on the data bus in response to the one or more driver-enable signals from the controller;

a receiver circuit configured to receive the first and second data via the data bus, the receiver circuit configured to latch the first and second data in response to the strobing clock signal generated by the controller;

a strobe clock signal line to propagate the strobing clock signal from the controller to the receiver circuit; and

a round-trip path comprising a return path for the strobing clock signal back to the controller;

wherein the controller is configured to enable the driver circuit to drive the first data on the data bus, generate the strobing clock signal propagated to the receiver circuit on the strobe clock signal line, receive the strobing clock signal on the round-trip path and, in response to receiving the strobe clock signal, enable the driver circuit to drive the second data on the data bus.

28. (Original) The multiple data rate memory device of claim 27, wherein the round-trip path is partially defined by the strobe clock signal line.

29. (Currently Amended) A multiple data rate memory device, comprising:

a driver configured to drive at least a first data and a second data;

a receiver coupled to the driver;

a controller coupled to the driver and configured to enable the driver to drive the first data and the second data;

a strobe clock signal line coupled between the receiver and controller and configured to propagate a strobe clock signal; and

a return clock signal line coupled at an output end to the controller and configured to propagate a return clock signal signaling the controller to enable the driver to drive the second data; wherein the return clock signal is timed off of the strobe clock signal.

30. (Original) The device of claim 29, wherein the strobe clock signal and the return clock signal have a period no longer than a period of an external clock signal received by the controller.

31. (Original) The device of claim 29, wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory.

32. (Original) A clocking circuit in a multiple data rate memory device, comprising:

a controller comprising a strobe clock signal output and a return clock signal input and configured to issue a first enable signal and a second enable signal, the first enable signal enabling a plurality of drivers to drive respective first data on respective data lines, and the second enable signal enabling the plurality of drivers to drive respective second data on their respective data lines;

a strobe clock signal line coupled to the strobe clock signal output; and

a return clock signal line coupled to the return clock signal input; wherein the strobe clock signal line defines an initial portion of a round-trip path and the return clock signal line defines a terminal portion of the round-trip path; and wherein the controller is configured to:

respond to an external clock signal by pulling a strobe clock signal to a first state on the strobe clock signal line and pulling the first enable signal to an active state;

receive a return clock signal on the return clock signal line a period of time after pulling the strobe clock signal to the first state, wherein the return clock signal is timed off of the strobe clock signal and indicates an assumed receipt of the strobe clock signal in the active state by receiving circuitry coupled to the respective data lines and configured to latch in the first and second data from the data lines in response to the strobe clock signal; and

respond to the received return clock signal by pulling the second enable signal to an active state.

33. (Original) The clocking circuit of claim 32, wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory.

34. (Original) The clocking circuit of claim 32, wherein the strobe clock signal line is coupled to the return clock signal line and to the receiving circuitry.

35. (Original) The clocking circuit of claim 32, wherein the receiving circuitry is configured to latch in the first data from the data lines in response to receiving the strobe clock signal in the first state and to latch in the second data from the data lines in response to receiving a transition of the strobe clock signal from the first state to a second state.

36. (Original) The clocking circuit of claim 32, wherein the return clock signal is a delayed instance of the strobe clock signal.

37. (Original) The clocking circuit of claim 32, wherein the strobe clock signal and the return clock signal are issued within a single period of an external clock signal.

38. (Original) The clocking circuit of claim 37, wherein the return clock signal is a delayed instance of the strobe clock signal.

39. (Original) A multiple data rate memory device, comprising:

a bidirectional data bus;

a first driver circuit coupled to the bus and configured to propagate a first data and a second data in a first direction along the bus;

a first receiver circuit coupled to an end of the bus opposite the first driver circuit and configured to latch the first and second data in response to a first strobe clock signal;

a second driver circuit coupled to the bus and configured to propagate a third data and a fourth data in a second direction along the bus;

a second receiver circuit coupled to an end of the bus opposite the second driver circuit and configured to latch the third and fourth data in response to a second strobe clock signal;

a first controller configured to enable the first driver circuit and to generate the first strobe clock signal;

a second controller configured to enable the second driver circuit and to generate the second strobe clock signal;

a first strobe clock signal line to propagate the first strobe clock signal from the first controller to the first receiver circuit;

a first round-trip path comprising a first return path for the first strobe clock signal back to the first controller;

a second strobe clock signal line to propagate the second strobe clock signal from the second controller to the second receiver circuit; and

a second round-trip path comprising a second return path for the second strobe clock signal back to the second controller.

40. (Original) The multiple data rate memory device of claim 39, wherein the first round-trip path is partially defined by the first strobe clock signal line and the second round-trip path is partially defined by the second strobe clock signal line.

41. (Canceled)

42. (Original) The multiple data rate memory device of claim 39, wherein the first strobe clock signal line comprises at least a portion of the second strobe clock signal line.